

REMARKS/ARGUMENTS

Claims 1, 4-19, 23-32, and 35-43 remain pending and claims 2, 3, 20, 21, 33 and 34 have been canceled without prejudice. Claim 31 has been amended, as recited hereinabove.

Claims 1, 4, 6-14 and 18-43 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Grieff et al. (US Patent No. 6,961,813) (hereinafter “Grieff”) in view of “SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA” and Utsunomiya et al. (U.S. Publication No.: 2003/0131166) (hereinafter “Utsunomiya”). It is believed that claims 1, 18 and 31 are patentable and all claims depending therefrom are therefore necessarily patentable over Grieff in view of “SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA” and Utsunomiya.

Claim 17 has been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Grieff et al. (US Patent No. 6,961,813) (hereinafter “Grieff”) in view of “SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA”, Utsunomiya et al. (U.S. Publication No.: 2003/0131166) (hereinafter “Utsunomiya”) and Shin et al. (U.S. Patent No. 7,154,905) (hereinafter referred to as “Shin”).

The combination of Utsunomiya and Grieff are not believed to render the claimed invention obvious and therefore unpatentable. Among other reasons, to combine the task file queue (in the main memory 16) of Utsunomiya with the disclosure of Grieff, which appears to be the basis of the subject rejection, the task file queue of Utsunomiya would have to be placed in the decoder 120 of Grieff because the latter is the only structure in Grieff that is being perceived as the task files of the claimed invention and to do otherwise would be re-design Grieff, which would no longer be the teaching of Grieff. To this end, Grieff still does not teach concurrent accessing of the device by multiple hosts, as in the claimed invention for reasons stated in previous-filed responses and during various Examiners’ Interview.

That is, even including, in the decoder 120 of Grieff, the task file queue of Utsunomiya will not allow the two host ports 130 and 132 to send commands, at any given time, to the drive via the dual port adaptor. The reasoning that while a host that has won arbitration is permitted to send a command to the dual port adaptor, the other host is prevented from sending commands to the dual port adaptor until the occurrence of a

particular event still holds true. One of the reasons for this is that the task file queue of Utsunomiya would be placed after the switch 110 of Grieff thereby preventing one host from sending commands to the device while the other host is doing so. The dual port adaptor of Grieff can not receive more than one command at a time, as noted in previous responses with which the Examiner seems to agree, because changing the CMD FIS 120 to become queue, such as that of Utsunomiya for holding more FISes will not alleviate the problem. In the information processing system of Utsunomiya, the HBA checks the BUSY status of the drive and if the drive is not BUSY, then the HBA sends command(s).

To place the host ports of Grieff into the information processing system of Utsunomiya would also not render the claimed invention obvious because while the task file queue of Utsunomiya includes more than one task file, only one host can access the main memory 16 and HBA 10 of Utsunomiya. There is no circuitry disclosed in Utsunomiya to allow for multiple host access. An information processing system comprising two instances of the system of Utsunomiya and the dual port adaptor of Grieff where each HBA is connected to a host port of dual port adaptor presents the same problem, as previously noted, with respect to prevention of one of the hosts from sending commands while another host is doing so. Furthermore since the host ports of Grieff 130 and 132 are Link Layer ports, the task file (which is at the application layer) queue of Utsunomiya can not be placed in host ports 130 and 132 of Grieff. Thus, it is believed that the combination forming the basis of the foregoing rejections are not operational relative to the claimed invention and therefore do not render the claimed invention obvious.

As a separate basis of patentability, combining Utsunomiya and Grieff are believed to be wrong because the latter discloses a system using the serial ATA (SATA) standard and the former discloses a system using the ATA standard and there is no suggestion of one as to standard of the other. These two standards are very different, as discussed during the Interview. Among their differences are: SATA uses a serial link that uses Gigabit technology and 8b/10b encoding for connectivity whereas ATA uses a parallel bus; and The architecture of SATA is based on four layers of communication: Application, Transport, Link, and Phy whereas only one layer (Application) of communication is used in ATA. To combine the foregoing standards would be to re-design the systems. The

claimed invention is directed to a system using the SATA standard, which is not disclosed by Utsunomiya.

Therefore, all independent claims 1, 18 and 31, are non-obvious and patentable over Grieff in combination with Utsunomiya and other cited references combined therewith. It is therefore also believed that all claims depending therefrom are patentable. Moreover, as all other rejections appear to combine Grieff and Utsunomiya, they are also believed to be moot in light of the foregoing arguments/remarks.

Reconsideration and allowance of claims 1, 4-19, 23-32, and 35-43 is hereby respectfully requested. Applicants submit that the subject application is now in condition for allowance and an early notice thereof is respectfully requested. Should any further amendment be required prior to passing the application to issue, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Respectfully submitted,
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